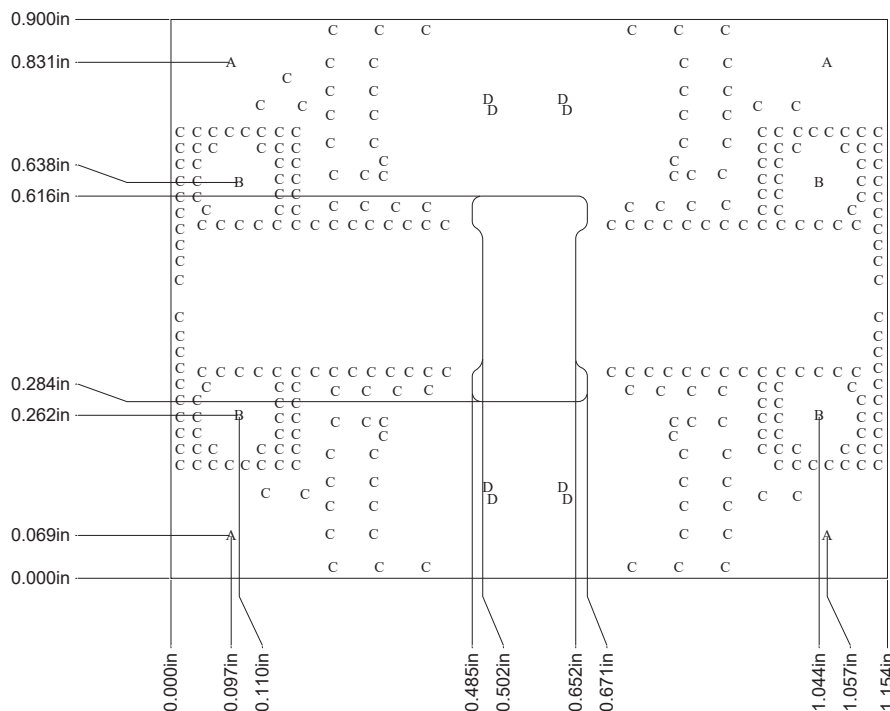


SUPPLIER MUST SEND EMAIL TO EVBHOLD@QORVO.COM IF JOB IS PLACED ON HOLD
SUPPLIER SHALL SEND A COPY OF FINAL WORKING GERBERS TO CEADS@QORVO.COM

NOTES: (UNLESS OTHERWISE SPECIFIED)

- BOARD FABRICATION METHODS MUST COMPLY WITH:
FABRICATE IN ACCORDANCE WITH IPC-6018B, per IPC-6011, CLASS 2.
- ARTWORK FORMAT: GERBER 274X
GERBER DATA SUPPLIED WITH DESIRED FINAL TRACE WIDTHS. PROCESS
COMPENSATION TRACE WIDTH ADJUSTMENTS TO BE DONE BY PCB FABRICATOR
- NUMBER OF LAYERS: 2 LAYERS
METAL 1 0.5oz. (Plus Plating)
CORE 1: TACONICS RF-35HTC, .005in. THICK
METAL 2 0.5oz. (Plus Plating)
SOLDERMASK TOP: LPI (LIQUID PHOTO-IMAGEABLE), GREEN OR LDI (LASER DIRECT IMAGEABLE),
GREEN. MAX FINISH THICKNESS OF SOLDERMASK TO BE 0.001in.
SILKSCREEN TOP: HIGH TEMPERATURE, NON-CONDUCTIVE, WHITE EPOXY BASED INK.
- FINISH PLATING:
A. METAL 1(TOP) AND METAL 4(BOTTOM):
ENEPIG (ELECTROLESS NICKEL, ELECTROLESS PALLADIUM, IMMERSION GOLD)
ENEPIG PLATING POST SOLDERMASK (ONLY ON OPENINGS)
- FINISHED BOARD THICKNESS: (0.009in) ±.003IN.
- COPPER IS PULLED BACK PER GERBER DATA FROM EDGE OF BOARD ON METAL 1 (TOP)
AND METAL 2 (BOTTOM) EXCEPT AROUND CONNECTOR AREA.
- TOLERANCE: PC BOARD OUTLINE:
A. PC BOARD OUTLINE: ±0.002in.TOLERANCE AND IS CRITICAL TO RF PERFORMANCE
B. POSITION OF INTERNAL CUTOOUT RELATIVE TO PCB OUTLINE ±.002.
- METAL TO EDGE IS NECESSARY. THE PRODUCT PERFORMANCE IS SIGNIFICANTLY
COMPROMISED WITH LARGE PULL BACKS. WE WILL ACCEPT BURRS.
- METALIZATION MUST BE FREE FROM CONTAMINATION AND DEBRIS.
- BURRS SHALL NOT EXCEED 0.002in.
- VIA PLATING/FILLING:
ALL PLATED THRU HOLES TO BE PLATED TO 0.0007in. MIN. THICKNESS.
- SINGULATION: EXTERNAL OUTLINE AND INTERNAL CUTOUTS ARE TO BE COMPLETED
VIA OPTICAL (LENZ) ROUTING OR LASER. LASER ROUTING IS AUTHORIZED ONLY IF IT
YIELDS A WIRE-BONDABLE SURFACE ADJACENT TO THE LASER-SAWN EDGE.
- FINISHED Cu THICKNESS TO BE .0018 ± .0005.
- CONDUCTOR WIDTHS AND SPACING TO BE WITHIN 0.001in. OF CAD DATABASE.
- SOLDERMASK IN PLATED-THRU HOLES IS ACCEPTABLE AS LONG AS IT DOES
NOT EXIST ON BACKSIDE OF BOARD.
- ALL HOLES TO BE LOCATED WITHIN ±0.003 OF CAD DATABASE.
- NO VENDOR MARKING ALLOWED EXCEPT DATE CODE FOR TRACEABILITY.
- BOARDS TO BE SINGULATED PER MECHANICAL 3 AND DELIVERED AS SINGLES
- NO ELECTRICAL TEST NEEDED.



* FOR MULTIPLE DRILL PROCESS JOBS SEE: *.DRL, *.DR1, *.DR2, etc.

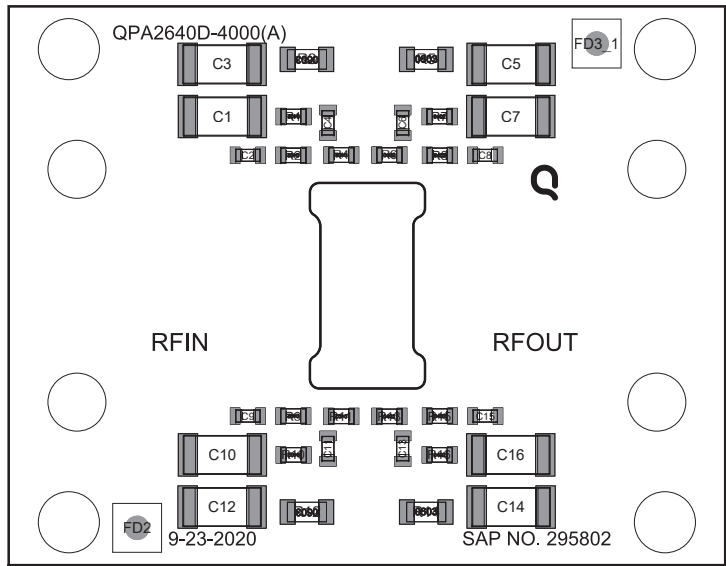
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES	SAP MATERIAL NUMBER: 295802	QORVO TITLE: QPA2640D EVALUATION PCB DESIGN PACKAGE	
	APPROVAL AND RELEASE RECORDS MAINTAINED IN PDE	DATE	
	DESIGNER: OMARRUFO ENGR: M.ROBERG	9/23/2020	
INTERPRET DRAWING PER ANSI/ASME Y14.5 - 2009	PDE CONTROLLED		
THIRD ANGLE PROJECTION DO NOT SCALE DRAWING			
SIZE B	DOCUMENT NUMBER: QPA2640D-4000	PROTOTYPE INSTANCE: N/A	REV. A
SHEET 1 OF 5		CAD: ALTIUM DESIGNER	SCALE: 2:1

Current Date & Time: 3/18/2021 12:29

FOR-001324 REV D

REFERENCE NOTE: Uses QPA2640D-4000[1] CAL SAP No. 295932

1. THE PCB WILL MOST LIKELY NOT BE FULLY POPULATED.



LAYER STACK LEGEND_SEE NOTE 3 FOR MATERIAL (COPPER THICKNESS IS @ FINISHED THICKNESS)

Material	Layer	Thickness	Dielectric Material	Type	Gerber
	SILKSCREEN_TOP			Legend	GTO
Surface Material	SOLDERMASK_TOP	0.0004in	Solder Resist	Solder Mask	GTS
Copper	METAL1_TOP	0.0018in		Signal	GTL
Core		0.0050in	TACONICS RF-35HTC	Dielectric	
Copper	METAL2_BOT	0.0018in		Signal	GBL
Total thickness: 0.0090in					

Drill Table (HOLE SIZES ARE DRILLED SIZE)

Symbol	Count	Hole Size	Plated	Drill Layer Pair
D	8	10.00mil(0.25mm)	Plated	METAL1_TOP - METAL2_BOT
C	276	15.00mil(0.38mm)	Plated	METAL1_TOP - METAL2_BOT
B	4	95.00mil(2.41mm)	Plated	METAL1_TOP - METAL2_BOT
A	4	100.00mil(2.54mm)	Plated	METAL1_TOP - METAL2_BOT
292 Total				

SIZE	DWG. NO.		PROTOTYPE	REV.
B	QPA2640D-4000		INSTANCE:	A
SHEET 2 OF 5	CAD: ALTIUM DESIGNER		SCALE:	2:1

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